Remarks

Upon entry of the foregoing amendment, claims 1-10 are pending in the application, with claims 1, 5, 8, and 10 being the independent claims. Claims 1, 3, 5, 6, 7, 8, and 10 are amended to correct minor informalities. These changes are believed to introduce no new matter, and their entry is respectfully requested.

The specification is also amended to correct minor typographical errors and to correct a reference number identifying the multiplexor to be consistent with the drawings as originally filed. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

The current Office Action states on page 2 that claims 1-3, 5-7, 8, and 10 are rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Pat. No. 6,199,154 B1 to Witt (hereinafter, "Witt"). Applicants respectfully disagree and traverse this rejection.

On page 2, paragraph 3(a), the Office Action considers the plurality of mappers as equivalent to "cache entries 16" in Figure 7 of Witt. To the contrary, the entries of L0 I-cache 16 of Witt are not mappers as defined in the present specification "for mapping an instruction of said instruction set to a predetermined instruction width format (PIWF) configuration" as recited in amended claim 1, for example. Rather, L0 I-cache 16 of Witt is

simply a cache similar to the traditional cache/cache controller configuration shown in Figure 1 of the present specification, minus mapper 120.

The Office Action appears to consider "mapping" as the equivalent of building the cache entries of a cache, for example with the tag, predecode data, and instruction byte of the cache entries shown in Figure 7 of Witt. The building of cache lines is discussed in the present specification, for example, in paragraph 20. However, the building of cache lines is not "mapping" as defined in the specification. Mapping, as defined in the present specification, is the conversion of an instruction "to a predetermined instruction width format ("PIWF") that is sufficiently wide to, and does, accommodate two or more instruction sets." (See the first sentence of paragraph 15 of the present specification.) The mapping of an instruction, as exemplified in the present specification, *occurs to* an instruction portion of a cache entry, such as, perhaps, a cache entry shown in the L0 I-cache 16 of Figure 7 of Witt. See, for example, paragraphs 24-30 of the present specification, which describes a traditional serial mapping system shown in Figure 1. In this example, as well as in the example embodiments that follow in the specification, the mapping occurs *after* cache entries, similar to those cache entries of Figure 7 of Witt, are already in existence.

Furthermore, according to Witt, the "predecode information generated by predecode unit 12 is stored in L1 I-cache 14" (Witt, col. 5, line 67 - col. 6, line 2) and "[c]ache storage 100 [of L0 I-cache 16] is coupled to receive a prefetched cache line from L1 I-cache 14...." (Witt, col. 25, lines 44-46). Witt does not teach any instruction-conversion occurring between the cache entries of the L1 I-cache 14 and the cache entries of the L0 I-cache 16. The building of cache entries as depicted in Figure 7 of Witt, which appears to simply be the passing of a cache line from the L1 I-cache to the L0 I-cache, is not the "mapping [of] an

instruction of said instruction set to a predetermined instruction width format (PIWF) configuration" as required in amended claim 1. Moreover, the start bit / boundary information of Witt's predecode data does not provide "mapping [of] an instruction of said instruction set to a predetermined instruction width format (PIWF) configuration" as required in amended claim 1. Thus, the L0 I-cache 16 is not a mapper as defined in the present application. Still further, even if we assume for purposes of argument that Witt's predecode unit 12 is a mapper, the predecode unit still does not constitute a "plurality of mappers" and does not "[map] an instruction of said instruction set to a predetermined instruction width format (PIWF) configuration" as required in claim 1.

For at least the reasons discussed above, claim 1 and the claims depending therefrom are believed to be allowable. Thus, Applicants respectfully request that the Examiner reconsider and withdraw the rejection(s) of these claims.

Claims 8 and 10 each include a "plurality of mappers" with recitation similar to that quoted above for claim 1. Thus, for at least the reasons discussed above for claim 1, claims 8 and 10, and the claims depending therefrom, are also believed to be allowable. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the rejection(s) of these claims as well.

Amended method claim 5 includes the features of "reading instructions of said instruction set from an instruction cache into a plurality of mappers..." and "mapping each instruction of said instruction set to a corresponding PIWF configuration," which correspond to the features discussed above in apparatus claims 1, 8, and 10. Thus, for at least the reasons discussed above for claims 1, 8, and 10, claim 5 and the claims depending therefrom, are also

believed to be allowable. Therefore, Applicants respectfully request that the Examiner also reconsider and withdraw the rejection(s) of these claims.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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